CLAIMS

What is claimed is:

1. A buffer management system (100), comprising: a buffer memory (200), and a controller (150), operably coupled to the buffer memory (200), that is configured to partition the buffer memory (200) into a plurality of independent buffers (220-223), dependent upon a partition parameter that determines a quantity of the plurality, wherein each buffer of the plurality of independent buffers (220-223) has a buffer-size that is an integer power of two, to facilitate circular-access to the buffer.

2. The buffer management system (100) of claim 1, wherein the controller (150) is configured to include a circular-increment function that requires only an address-increment function and a bit-overwrite function to effect a circular-increment of a pointer to a select buffer of the plurality of independent buffers (220-223).

3. The buffer management system (100) of claim 1, wherein the buffer-sizes of the plurality of independent buffers (220-223) are equal.

4. The buffer management system (100) of claim 1, wherein the controller (150) is further configured to allocate the plurality of independent buffers (220-223) among a plurality of source-destination paths.

5. The buffer management system (100) of claim 1, wherein the controller (150) is further configured to provide a write-interface (130) and a read-interface (140) to one or more applications, the write-interface (130) requiring only an identification of data to be stored and an identification of a select buffer of the plurality of independent buffers (220-223) to store the data, and the read-interface (140) requiring only the identification of the select buffer.

6. The buffer management system (100) of claim 1, wherein the buffer memory (200) is addressed by an M-bit address, each buffer of the plurality of independent buffers (220-223) is indexed by an N-bit index that forms a set of N most-significant-bits of the M-bit address, and the size of each buffer is at least 2^{M-N}.

7. A method of managing a buffer memory (200), comprising: receiving a partition parameter, partitioning the memory buffer into a plurality of independent buffers (220-223), wherein the plurality is determined from the partition parameter, and a size of each buffer of the plurality of independent buffers (220-223) is an integer power of two, thereby facilitating circular-addressing of each buffer.

8. The method of claim 7, wherein the sizes of the plurality of independent buffers (220-223) are equal.

9. The method of claim 7, further including providing circular-addressing for each buffer, wherein the circular-addressing includes: incrementing an address to the buffer memory (200), and overwriting select bits of the address, corresponding to an index to the buffer within the buffer memory (200).

10. The method of claim 7, further including: providing a write-interface (130) that requires only an identification of data to be stored and an identification of a select buffer of the plurality of independent buffers (220-223) to store the data, and providing a read-interface (140) that requires only the identification of the select buffer.

11. The method of claim 7, wherein the buffer memory (200) is addressed by an M-bit address, each buffer of the plurality of independent buffers (220-223) is indexed by an N-bit index that forms a set of N most-significant-bits of the M-bit address, and the size of each buffer is at least 2^{M-N}.

12. An integrated circuit, comprising a buffer memory (200), and a controller (150) that includes write control logic (130), and read control logic (140), wherein the controller (150) is configured to partition the buffer memory (200) into a plurality of buffers (220-223), based on a partition parameter that is provided to the controller (150), each buffer of the plurality of buffers (220-223) having a size that is an integer power of two, and the write control logic (130) and read control logic (140) are each configured to facilitate use of each buffer as a circular buffer.

13. The integrated circuit of claim 12, wherein the sizes of the plurality of buffers (220-223) are equal.

14. The integrated circuit of claim 12, wherein the use of each buffer as a circular buffer requires circular-addressing, and the controller (150) is configured to effect the circular-addressing via an incrementer that is configured to increment an address to the buffer memory (200), and a bit masker that is configured to overwrite select bits of the address, corresponding to an index to the buffer within the buffer memory (200).

15. The integrated circuit of claim 12, wherein the write control logic (130) effects a storage of a data value to a select buffer of the plurality of buffers (220-223) based only on an identification of the data value and an identification of the select buffer, and the read control logic (140) effects a retrieval of the data value based only on the identification of the select buffer.

16. The integrated circuit of claim 12, wherein the buffer memory (200) is addressed by an M-bit address, each buffer of the plurality of independent buffers (220-223) is indexed by an N-bit index that forms a set of N most-significant-bits of the M-bit address, and the size of each buffer is at least 2^{M-N}.